

#14/S-10-04
B/ u Jones



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Serial No.: 09/697,305

Filed: October 27, 2000

Group Art Unit: 2133

Examiner: Joseph D. Torres

For: FAULT DETECTING METHOD AND LAYOUT METHOD
FOR SEMICONDUCTOR INTEGRATED CIRCUIT

AMENDMENT

RECEIVED

MAY 05 2004

Technology Center 2100

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Prior to examination of the above-identified continuing application, please amend the claims in the application as follows: